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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,385	08/26/2003	Mitsunori Tsujino	67161-076	2048

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McDermott, Will & Emery
600 13th Street, N.W.
Washington, DE 20005-3096

EXAMINER	
GLENN, KIMBERLY E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,385	TSUJINO ET AL.	
	Examiner	Art Unit	
	Kimberly E Glenn	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,9 and 10* is/are rejected.

7)☒ Claim(s) *2-4 6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al US Patent 5,825,698.

Kim et al disclose in figure 2 a circuit comprising a transistor MN2 connecting a first internal node to a first power supply node with a first power supply potential (ground) in response to a first control signal (PORESET); a master fuse provided on a path between a second power supply node provided with a second power supply potential (Vcc) which is different from said first power supply potential (ground) and said first internal node, and storing a conductive state in a non-volatile manner; and a latch circuit 10 for holding a logic value corresponding to a potential of said first internal node; wherein said latch circuit includes a inverter 11 having an input connected to said first internal node, and driving unit (MP2 MP1 MN1) driving said first internal node to said power supply potential in accordance with an output of the inverter and said driving unit has a drivability variable in response to a second control signal (DESELROW).

Kim et al further disclose a pulse generator connected to the MN2 transistor. Transistor MN2 is controlled by a pulse of the PORESET signal having a predetermined

width that is generated by power up pulse generator 30 upon power-up of the semiconductor memory device. Column 1; lines 20 through column 2; line 23 and column 4; lines 19 through 47.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Bohm et al US Patent 6,353,562.

Bohm et al disclose in figure 4 a circuit comprising a transistor connecting a first internal node to a first power supply node with a first power supply potential (V1) in response to a first control signal (FH); a fuse F provided on a path between a second power supply node provided with a second power supply potential (ground) which is different from said first power supply potential (V1) and said first internal node, and storing a conductive state in a non-volatile manner; and a circuit for holding a logic value corresponding to a potential of said first internal node and a transistor provided in series with the fuse between the internal node and the second power supply node and connected to a control signal (FL). Inherently, the transistor connected in series with the fuse will act a resistance. Column 5; line 1 through 42.

Allowable Subject Matter

Claims 2-4 and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kato US Patent 6,465,818,Vasenko et al US Patent 6,144,591, Gilliam US Patent 5,566,107 and Sredanovic et al US Patent 6,084,803.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly E Glenn whose telephone number is (571)-272-1761. The examiner can normally be reached on Monday-Friday 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BENNY T. LEE
PRIMARY EXAMINER
ART UNIT 2817

Kimberly E Glenn
Examiner
Art Unit 2817

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